

Applicant : Martin J. Edwards  
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Attorney Docket: 14509-0131US1 / P080487SEXCLUS

Amendments to the Drawings:

The attached replacement sheet of drawing includes changes to FIG. 2 and replaces the original sheet including FIG. 2.

Attachments following last page of this Amendment:

Replacement Sheet (1 page)

### REMARKS

The comments of the Applicant below are each preceded by related comments of the Examiner (in small, bold type)

**Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).**

FIG. 2 has been amended.

**The abstract of the disclosure does not commence on a separate sheet in accordance with 37 CFR 1.52(b)(4). A new abstract of the disclosure is required and must be presented on a separate sheet, apart from any other text.**

A new abstract has been provided on a separate sheet.

**The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.**

The title has been amended.

**The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.**

Applicant notes that the guidelines are suggested but not required by the patent rules.

**Claims 1-5, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Edwards et al (US 2002/0054005).**

Consider claim 1, Edwards discloses an active matrix display device comprising a row and column array of picture elements (see fig. 1), sets of row and column address conductors (18, 19) for selecting rows of picture elements and providing data signals to the picture elements of a selected row respectively (see fig. 1), drive means (21, 23, 25) for supplying selection signals and multi-bit digital data signals respectively to the set of row address conductors and the set of column address conductors (see fig. 1, elements 21, 23, and 25), and in which the multi-bit digital data signals supplied to the column address conductors are converted into analogue voltage levels for use by the picture elements by a plurality of serial charge redistribution digital to analogue conversion means (see fig. 3 and par. [0023]-[0024]), each conversion means (30A, 30B, 30C) comprising at least first and second capacitances interconnectable by at least one conversion switch (see fig. 3) and between which charge is shared (see fig. 3), and in which the first and second capacitances of

**a conversion means are provided by the capacitances of two column address conductors (see fig. 7, where the capacitors of column 19a and 19b are shared), wherein the drive means is arranged to alternate the supply of data signals to the first and second column address conductors of each conversion means (see par. [0028] and fig. 4, where the converted voltage is represented on one of the column electrodes only and switch A and B are switched alternately).**

Edwards (U.S. patent publication 2002/0054005) does not describe and would not have made obvious a drive means that is arranged to alternate the supply of data signals to the first and second column address conductors of each conversion means, as recited in claim 1.

In Edwards, the output amplifier 33 can either drive only the sub-column electrode 19a (when switch A is closed and switch B is open), or both the sub-column electrodes 19a and 19b (when both switches A and B are closed). See FIG. 3 of Edwards. If the Examiner contends that the sub-column electrodes 19a and 19b of Edwards correspond to the first and second column address conductors of claim 1, then Edwards does not disclose or suggest that the column drive circuit 25 alternate the supply of data signals to the sub-column electrode 19a and the sub-column electrode 19b.

What Edwards discloses is that the column drive circuit 25 transfers the digital data to the column electrode 19a (paragraph [0028], lines 7-11) and perform a conversion process by controlling switches 31A, 31B, and 31C to allow charge sharing between the capacitors associated with the column electrodes 19a and 19b. Edwards discloses that, when the final charge sharing is completed, the converted voltage is present on one of the column electrodes only, and a subrow electrode (either 18a or 18b) can be selected to transfer the converted voltage to half of the display elements in a row.

Applicant notes that, in Edwards, it is after the final charge sharing will the converted voltage be present on one of the column electrodes only. The converted voltage is not provided by the column drive circuit 25. Therefore, Edwards does not disclose or suggest a drive means that is arranged to alternate the supply of data signals to the first and second column address conductors of each conversion means, as recited in claim 1.

**Consider claim 2, Edwards discloses the column address conductor (19) of a conversion means to which the data signals are applied is changed after one or more complete multi-bit signal conversions performed by the conversion means (see par. [0028]).**

In Edwards, the column drive circuit 25 supplies data signals to the column electrode 19a, and does not supply data signals to the column electrode 19b after one or more complete multi-bit signal conversions. If the Examiner contends that the column electrodes 19a and 19b correspond to the first and second column address conductors of claim 1, then Edwards does not disclose or suggest changing the column address conductor of a conversion means to which the data signals are applied after one or more complete multi-bit signal conversions.

**Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards et al (US 2002/0054005) in view of Nakajima et al (US 6157358).**

**Consider claim 6, Edwards discloses the limitation of claim 1. Edwards does not specifically disclose the polarity of the voltage provided to the picture elements is inverted periodically, and wherein the alternation of the column conductors (19) of a conversion means to which a data signal is applied to generate the analogue voltage level for a given picture element is synchronized with the inversion of the picture element voltage. Nakajima discloses the polarity of the voltage provided to the picture elements is inverted periodically, and wherein the alternation of the column conductors (19) of a conversion means to which a data signal is applied to generate the analogue voltage level for a given picture element is synchronized with the inversion of the picture element voltage (see fig. 1 and col. 3 lines 39-49).**

**It would have been obvious to one skilled in the art at the time the invention was made to modify the invention of Edwards, and have discloses the polarity of the voltage provided to the picture elements is inverted periodically, and wherein the alternation of the column conductors (19) of a conversion means to which a data signal is applied to generate the analogue voltage level for a given picture element is synchronized with the inversion of the picture element voltage, as taught by Nakajima, thus preventing crosstalk.**

Edwards does not describe and would not have made obvious alternation of the column conductors of a conversion means to which a data signal is applied, as recited in claim 6. Rather, Edwards discloses a column drive circuit 25 that transfers digital data to a column electrode 19a (paragraph [0028], lines 7-11) and performs a conversion process by controlling switches 31A, 31B, and 31C to allow charge sharing between the capacitors associated with the column electrodes 19a and 19b. Edwards does not disclose or suggest alternation of the column conductors to which a data signal is applied.

What is missing in Edwards is also not disclosed or suggested in Nakajima. Although Nakajima discloses that a DA converter 19 can drive one of two columns depending on switch selection, the two columns being driven by the DA converter 19 are not two column conductors of a conversion means. Nakajima does not disclose or suggest a conversion means. Therefore, neither Edwards nor Nakajima discloses or suggests altering the column conductors of a conversion means to which a data signal is applied, let alone synchronizing the alternating of the column conductors with an inversion of a picture element voltage, as recited in claim 6.

#### New Claim 11

Edwards does not describe and would not have made obvious “when data signals are supplied to the first column address conductor, the data signals are not supplied to the second column address conductor, and when data signals are supplied to the second column address conductor, the data signals are not supplied to the first column address conductor,” as recited in claim 11.

In Edwards, the output amplifier 33 can either drive only the sub-column electrode 19a (when switch A is closed and switch B is open), or both the sub-column electrodes 19a and 19b (when both switches A and B are closed). See FIG. 3 of Edwards. Edwards does not disclose or suggest that when data signals are supplied to the sub-column electrode 19a, the data signals are not supplied to the sub-column electrode 19b, and when data signals are supplied to the sub-column electrode 19b, the data signals are not supplied to the sub-column electrode 19a. In Edwards, the data signals cannot be supplied to the sub-column electrode 19b without also being supplied to the sub-column electrode 19a.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Any circumstance in which the applicant has addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner. Any circumstance

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in which the applicant has made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims. Any circumstance in which the applicant has amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Please apply \$1,110 for the Petition for Extension of Time fee and any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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